MN-30-520-X-S04, 30 – 520 MHz, 1 Watt, Tunable Bandpass Filter, MINI-ERF®

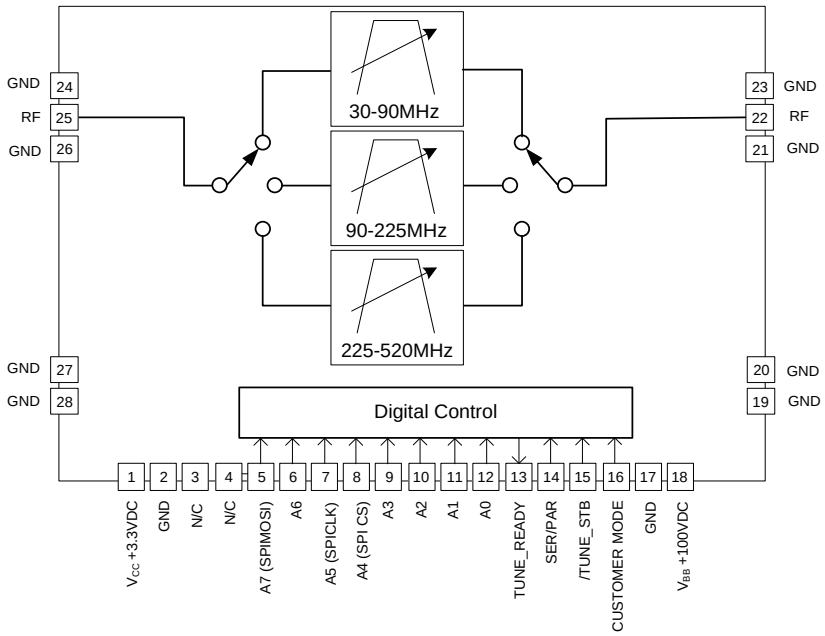
Typical Applications

- Military Radios
- Military Radar
- SATCOM
- Test and Measurement Equipment
- Industrial and Medical Equipment

Features

- 1 Watt CW continuous power handling
- +40 dBm IIp3 (typ.)
- Low IL (5.5 dB typ., 4% filter)
- 22 dB selectivity @ +/-10%, (4.7% filter)
- Fast Tune Time (15 µs, typ.)

Functional Diagram



Description

The MINI-ERF® is a low-cost, miniature, high-performance tunable band pass filter. The MINI-ERF® uses PIN diodes to deliver high filter performance while fitting in a 1.75” x 2.40” x 0.387” package. Serial or parallel tuning interfaces are selectable. All MINI-ERF® filters are fully tuned and tested by POLE/ZERO® for convenience and ease of use.

1.0 Ordering Information

Table 1. Ordering Options

Series	-	Frequency Range (MHz)	-	% Bandwidth (3 dB)	-	Package
MN	-	30-520	-	4	-	S04
				7		
				10		

Note: Options may be limited to particular frequency bands and/or configurations. Consult Pole/Zero for your application.

Example product number: MN-30-520-7-S04

2.0 Pinout and Functional Information

2.1 Pinout

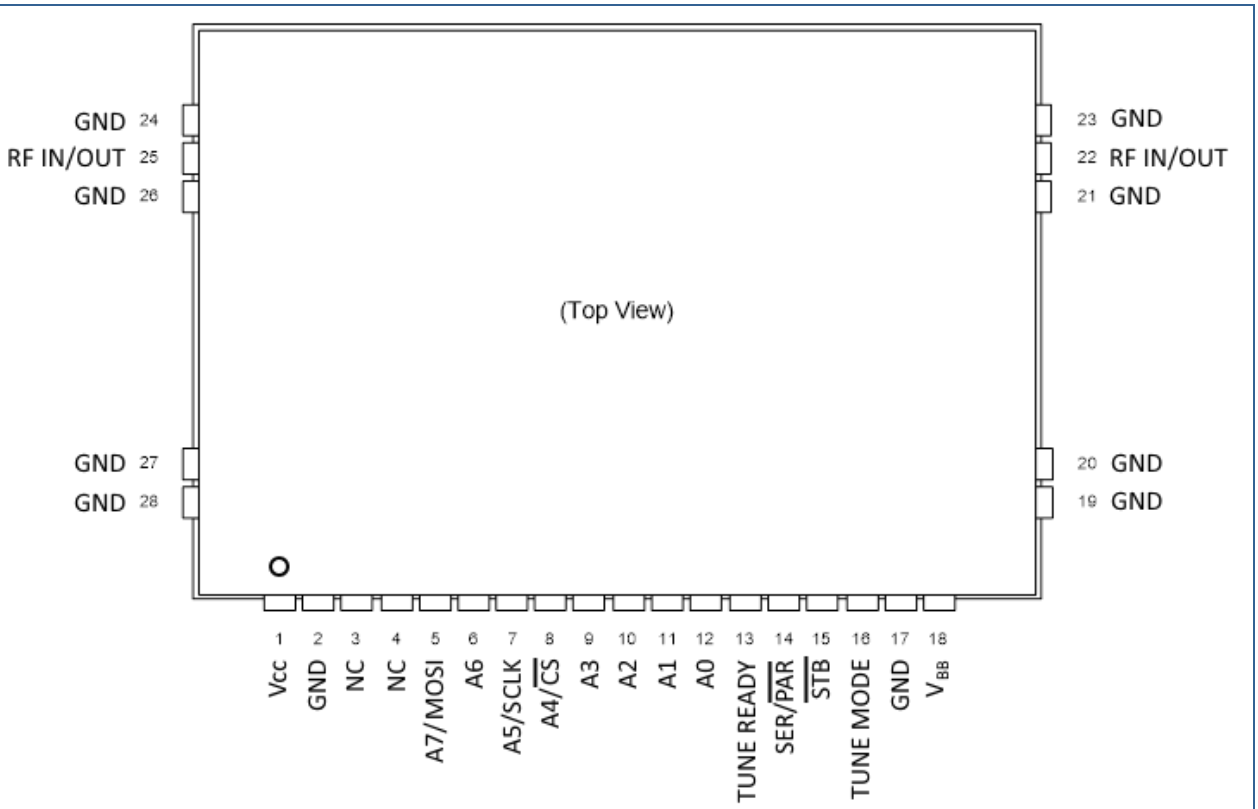


Figure 1. Pin Configuration

2.2 Pin Description

Table 2. Pin Functions and Descriptions

Pin Number	Label	Description
1	Vcc	Supply Voltage Input: 3.135 V ≤ V_{CC} ≤ 3.6 V.
2, 17, 19, 20, 21, 23, 24, 26, 27, 28	GND	Digital and Analog Ground.
3, 4	NC	No Connect – Factory use only pins. Shorting or connecting these pins may affect the performance and functionality of the filter. Leave these pins floating.
22, 25	RF IN/OUT	RF Signal Input or Output.
5	A7	Parallel Data A7 (MSB) – In Parallel interface mode, data is latched on the rising edge of $\overline{STB}$ and indicates which frequency the filter should tune to (A7 = MSb, A0 = LSb). (This pin is internally pulled to VCC with a 27 kΩ resistor.)
	MOSI	Serial Tune Interface Master Output Slave Input – Data is applied to MOSI for transferring a tune command to the device. Each bit of data is latched on the rising edge of SCLK. The filter accepts tune command lengths of 16-bits. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
6	A6	Parallel Data A6. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
7	A5	Parallel Data A5. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
	SCLK	Serial Tune Interface Clock – SCLK is used to clock in the tune word. Data is latched on the rising edge of SCLK. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
8	A4	Parallel Data A4. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
	$\overline{CS}$	Serial Tune Interface Chip Select – The master transmits logic '0' for the desired filter using the chip select line. When $\overline{CS}$ is taken low, the control circuitry wakes up and the filter is ready for a new tune command. When the entire tune word has been loaded into the filter $\overline{CS}$ is taken high to indicate the tune command is complete. ***For proper operation in Serial mode, tie this pin directly to $\overline{STB}$ (pin 15).*** (This pin is internally pulled to VCC with a 27 kΩ resistor.)
9	A3	Parallel Data A3. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
10	A2	Parallel Data A2. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
11	A1	Parallel Data A1. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
12	A0	Parallel Data A0 (LSB). (This pin is internally pulled to VCC with a 27 kΩ resistor.)
13	TUNE READY	Tune Ready Indicator – This pin normally remains low. When $\overline{CS}$ and/or $\overline{STB}$ is taken low to initiate a tune in either SPI or Parallel tune modes, the TUNE READY pin transitions high to indicate the filter is ready to receive the SPI or Parallel data. After data has been shifted in via the tune interface, the TUNE READY pin will transition back low indicating that the tune process is finished.
14	SER/$\overline{PAR}$	Serial/Parallel Command Interface Selection – Leaving SER/$\overline{PAR}$ floating or pulled to V_{CC} will enable the SPI (serial) tune command interface. Keeping SER/$\overline{PAR}$ pulled to GND will enable the parallel tune command interface. A power cycle is required to change modes. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
15	$\overline{STB}$	In Serial interface mode – $\overline{STB}$ wakes the controller circuitry on a low transition. ***For proper operation in SPI mode, tie this pin directly to $\overline{CS}$ (pin 8).*** In Parallel interface mode, when $\overline{STB}$ is taken low, the control circuitry wakes up and data is ready to be sent on A7-A0. When $\overline{STB}$ is transitioned high, the MSB of parallel data is latched. $\overline{STB}$ should be taken low again while the LSB is loaded on the data port. When $\overline{STB}$ is transitioned high for the second time, the LSB of parallel data is latched and the filter is commanded to the frequency specified by the parallel data interface. (This pin is internally pulled to VCC with a 27 kΩ resistor only when used in parallel mode.)
16	TUNE MODE	Leave this pin floating or pull to V_{CC} to enable legacy tune mode[1] – Pulling this pin low is not supported at this time and is reserved for future use. The MINI-ERF® will not operate correctly if this pin is pulled low. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
18	V_{BB}	High Bias Supply Voltage Input: +100 VDC for optimum performance.

[1] Contact Pole/Zero for more information on future/custom interface requirements.

3.0 Specifications

3.1 Absolute Maximum Ratings[2]

Voltages are referenced to GND (ground = 0V). Operating at room temperature (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	-	-0.3	4	V
V_{BB}	High supply voltage	-	-0.5	105	V
V_I	Input voltage	On all digital interface input pins	-0.5	Vcc + 0.5	V
V_O	Output voltage	On all digital interface output pins	-0.5	Vcc + 0.5	V
I_{OH}/I_{OL}	Digital interface pin sink/source current	-	-25	25	mA
I_O	Output current	-	-	200	mA
P_{INBAND}	In-band RF input power level	Signal is in passband $f_0 = 30 - 520\ MHz$	-	32	dBm
$P_{OUTBAND}$	Out-of-band RF input power level	-	-	33	dBm
T_{RATE}	Maximum tune rate (frequency hopping)	-	-	2	kHz

3.2 Handling Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
T_S	Storage temperature	-	-40	125	°C

3.3 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{CC}	Supply voltage	-	3.135	3.3	3.6	V
V_{BB}	High supply voltage	-	90	100	105	V
P_{IN}	Maximum RF input power for linear operation	Signal is in passband	-	-	30	dBm
T_A	Ambient temperature	-	-40	-	85	°C

3.4 Electrical Characteristics

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_{CC_STATIC}	V_{CC} current consumption, statically tuned	At nominal V_{CC} voltage	-	100	290	mA
I_{CC_HOP}	V_{CC} current consumption, hopping	Nominal V_{CC}, hopping at 2 kHz	-	-	290	mA
V_{BB}	High supply voltage	-	90	100	105	V
I_{BB_STATIC}	V_{BB} current consumption, statically tuned	At nominal V_{BB} voltage	-	1.4	2.5	mA
I_{BB_HOP}	V_{BB} current consumption	Nominal V_{BB}, hopping at 2 kHz	-	-	17.5	mA
V_{IH}	Digital high level input voltage	On all digital interface input pins	0.7 * V_{cc}	-	-	V

[2] Maximum operating conditions before damage occurs.

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{IL}	Digital low level input voltage	On all digital interface output pins	-	-	0.3 * V_{cc}	V
I_{IH}/I_{IL}	Digital Interface pin input logic current	-	-25	-	+25	mA
F_{RANGE}	Tunable frequency range	-	30	-	520	MHz
Z_O	Input/output impedance	-	-	50	-	Ω
VSWR	Voltage Standing Wave Ratio	-	-	1.5:1	2.2:1	-
T_{TUNE}	Tune time	-	-	15[3]	-	µs
F_{DRIFT}	Center frequency drift over temperature	-	-40	-	-80	ppm/°C

3.5 Selection Guide:

Band	Suffix	3 dB %BW		Insertion Loss (IL) (dB)		Return Loss (dB)		Shape Factor Overall $\left(\frac{30\text{ dB}}{3\text{ dB}}\right)$		Selectivity (f_0 ± 10%) (dB)		Ultimate Selectivity ($2 * f_0$) (dB)[4]	IIP3 (dB)[5]	Noise Figure (dB)	
-	-	Avg	Max	Avg	Max	Avg	Min	Avg	Max	Avg	Min	Typical	Avg	Avg	Max
30 - 520	-4	4.7	5.4	5.2	7	14	8.52	6.5	7.1	22	19	65	40	IL	IL ± 1dB
	-7	7.2	8.2	3.5	5	14	8.52	6.5	7.1	16	14	65	40	IL	IL ± 1dB
	-10	10.2	11.0	2.7	4.0	18	8.52	6.5	7.1	11	9	60	40	IL	IL ± 1dB

[3] For an input signal of 0 dBm. Refer to section 6: Tune time for more information
[4] Typical performance, ultimate selectivity is not guaranteed.
[5] 2-Tone IIP3 measurement with tones at +24 dBm. Results with tone levels below +24 dBm may result in lower IIP3.

3.6 Typical Characteristics

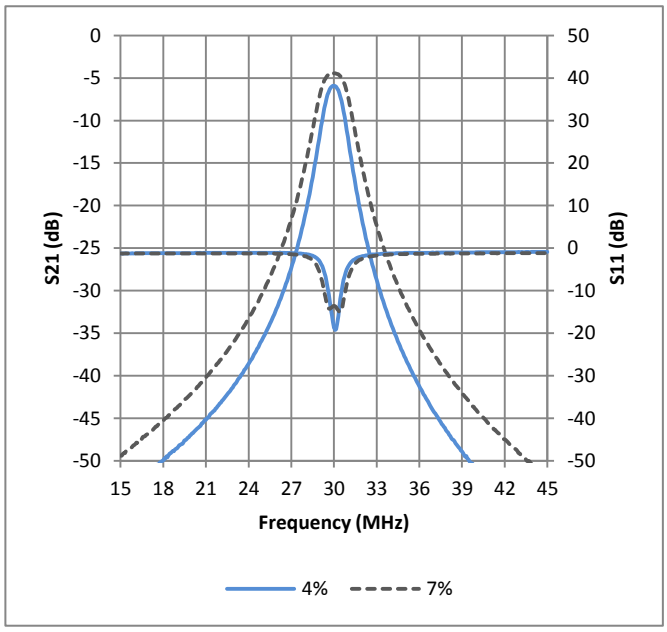


Figure 2. Filter response at 30 MHz

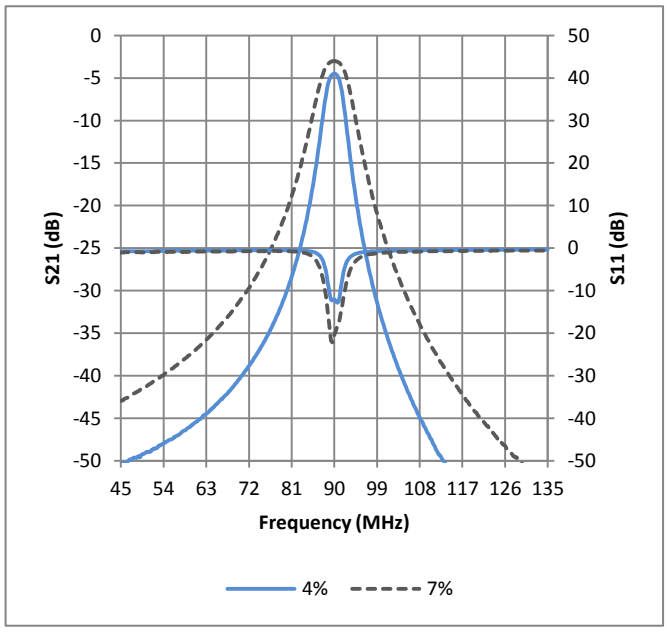


Figure 3. Filter Response at 90 MHz

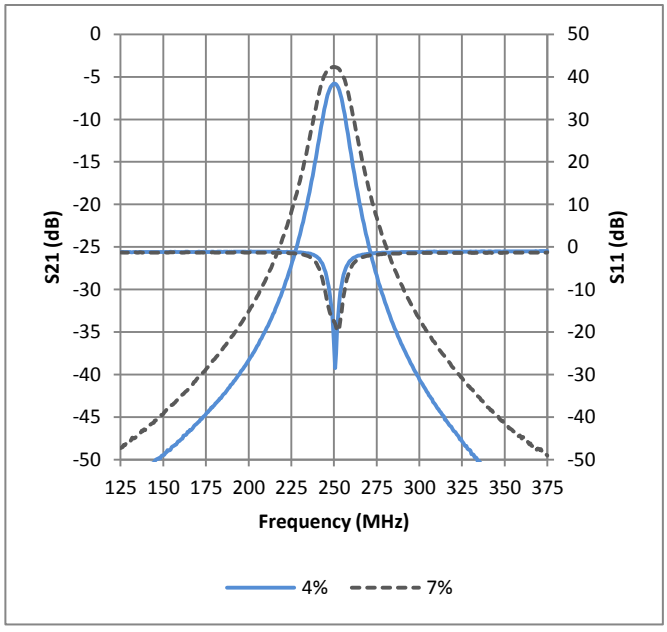


Figure 4. Filter Response at 250 MHz

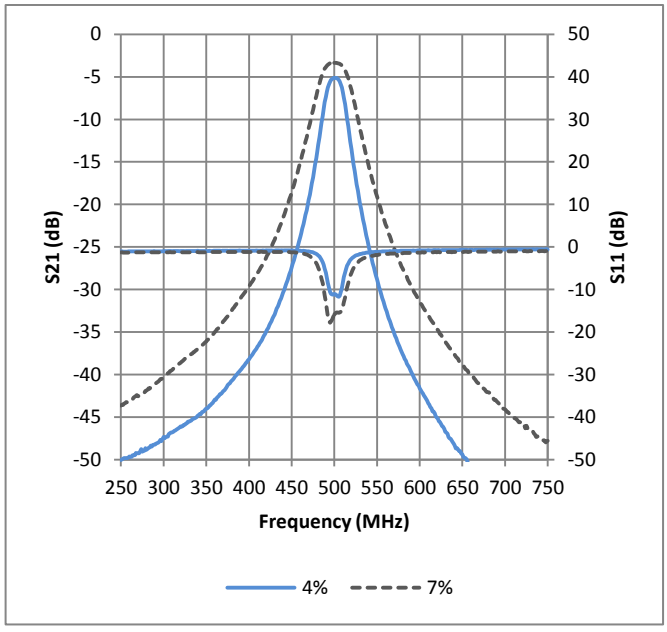


Figure 5. Filter Response at 500 MHz

3.7 Timing Requirements

3.7.1 SPI Interface Timing

The SPI tune command interface is a standard SPI interface with Mode = 0 (CPOL = 0, CPHA = 0). There are always 16 data bits regardless of the tune mode used. Any bits that do not affect the frequency offset of the filter should always be set to 0. The interface receives the data most significant byte and most significant bit first. The SPI interface can be used in legacy and bit weighted tune modes. The SPI interface is selected by leaving SER/$\overline{PAR}$ floating or pulled to V_{CC}. ***Pin J8 and J15 ($\overline{CS}$ & $\overline{STB}$) must be tied together externally for SPI mode to function properly.***

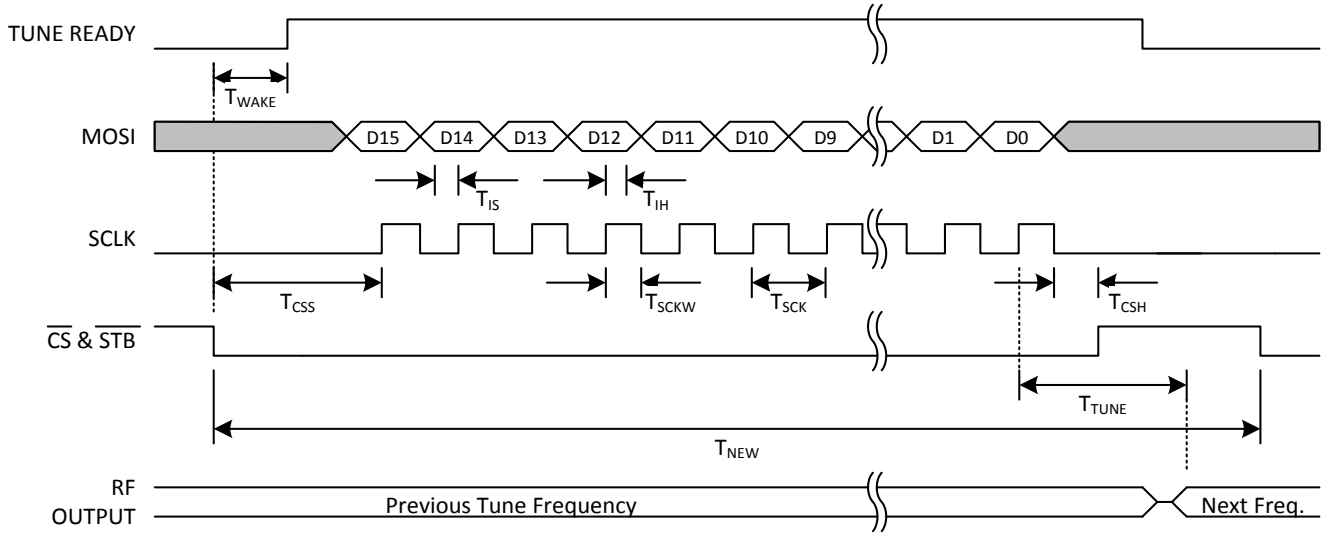


Figure 6. Serial Timing Diagram

Table 3. SPI Timing Characteristics

V_{CC} = 3.3 V +/-5%, GND = 0 V

Parameter	Parameter	Min.	Max.	Unit
T_{WAKE}	Wakeup Time – The amount of time from $\overline{CS}$ & $\overline{STB}$ transitioning low until TUNE READY transitions high.	-	6.5	µs
T_{CSS}	$\overline{CS}$ & $\overline{STB}$ Setup Time – The amount of time needed from when $\overline{CS}$ & $\overline{STB}$ transitions low until the first rising edge of SCLK.	6.8	-	µs
T_{IS}	MOSI Setup – The amount of time data needs to be present on MOSI before the rising edge of SCLK.	10	-	ns
T_{IH}	MOSI Hold – The amount of time data needs to be held on MOSI after the rising edge of SCLK.	40	-	ns
T_{SCK}	SCLK Period	143	-	ns
T_{SCKW}	SCLK Duty Cycle	$\frac{T_{SCLK}}{2}$	-	ns
T_{SCKF}	SCLK Fall Time (not shown in diagram)	-	1.6	µs
T_{SCKR}	SCLK Rise Time (not shown in diagram)	-	1.6	µs
T_{CSH}	$\overline{CS}$ & $\overline{STB}$ Hold Time – The amount of time $\overline{CS}$ & $\overline{STB}$ needs to remain low after the last falling edge of SCLK.	50	-	ns
T_{NEW}	New Command Delay – The amount of time between falling edges of $\overline{CS}$. This is the time between the start of new tune commands.	500	-	µs
T_{TUNE}	Time from the last rising edge of clock until the RF response reaches 90%.	-	21	µs

3.7.2 Parallel Interface Timing

The Parallel tune command interface is an 8-bit wide synchronous parallel interface with a two-byte load. There are always 16 data bits per parallel tune regardless of the tune mode used. Any bits that do not affect the frequency offset of the filter should always be set to 0. A7 is the most significant bit and A0 is the least significant bit. The Parallel interface can be used in legacy and bit weighted tune modes. Keeping SER/$\overline{PAR}$ pulled to GND will enable the parallel tune command interface.

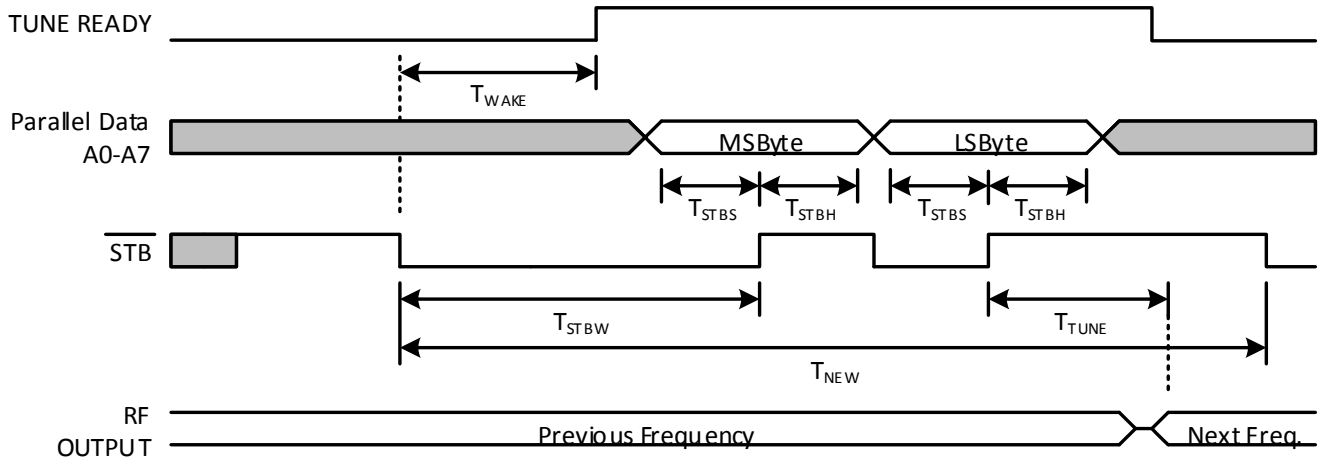


Figure 7. Parallel Timing Diagram

Table 4. Parallel Timing Characteristics

Symbol	Parameter	Min.	Max.	Unit
T_{WAKE}	Wakeup Time –The amount of time from $\overline{STB}$ transitioning low until TUNE READY transitions high.	-	6.5	µs
T_{STBW}	Strobe Wait Time – The amount of time needed to wait after $\overline{STB}$ transitions low before $\overline{STB}$ can transition back high to latch the most significant byte of the parallel tune command.	7.1	-	µs
T_{STBS}	Parallel Data Setup Time – The amount of time parallel data needs to be present and valid before $\overline{STB}$ transitions high.	300	-	ns
T_{STBH}	Parallel Command Hold Time – The amount of time the command data needs to be present and valid after $\overline{STB}$ transitions high.	300	-	ns
T_{NEW}	New Command Delay – The amount of time between subsequent first falling edges of $\overline{STB}$. This is the time between the start of new tune commands.	500	-	µs
T_{TUNE}	Time from the last rising edge of $\overline{STB}$ until the RF response reaches 90%.		21	µs

4.0 Functional Description

4.1 Legacy Tune Mode

Legacy tune mode is used the same way that the tune interface of a legacy ERF product is used. The tune word is a two-byte load with the first byte (MSB) being the band the filter should tune to, and the second byte (LSB) being the frequency offset in the chosen band. Legacy tune mode can be selected by leaving the TUNE MODE pin floating or pulled up to +3.3 V. The Legacy tune mode can be used in both serial and parallel modes.

Table 5. . Legacy Tune Word Properties

Symbol	Band	Value	Description
f_{MIN}	VHFL	30 MHz	Minimum Tunable Frequency. f_{MIN} is the absolute minimum frequency that the filter is capable of tuning to for the respective band.
	VHFH	90.54 MHz	
	UHF	226.18 MHz	
f_{MAX}	VHFL	90 MHz	Maximum Tunable Frequency. f_{MAX} is the absolute maximum frequency that the filter is capable of tuning to. Sending tune commands greater than the maximum tunable frequency will result in an invalid tune condition. The frequency response of an invalid tune is unknown. Normal frequency response will return on the next valid tune command. Varies depending on the band.
	VHFH	225 MHz	
	UHF	520 MHz	
f_{STEP}	VHFL	0.24 MHz	Tune step size. f_{STEP} is the minimum spacing between adjacent tune commands.
	VHFH	0.54 MHz	
	UHF	1.18 MHz	
f_{COM}	-	$round\left(\frac{(f_{DESIRED} - f_{MIN})}{f_{STEP}}\right)$	Commanded Frequency. f_{COM} is the commanded frequency that is sent over the SPI or parallel tune interface. The command can be calculated by subtracting f_{MIN} from the desired frequency for the particular band, dividing the result by the f_{STEP} of that band, and then rounding to the nearest integer command. The formula is used to select the closest possible frequency to the desired tune word. If the next lowest tune word is desired, replace the round operation with floor and if the next highest tune word is desired replace the round operation with ceil.

Table 6. Legacy Tune Word Format

Tune Word Format															
(MSb) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	(LSb) 0
0	0	0	0	0	0	Band Bits		Commanded Frequency							

5.0 Detailed Description

5.1 Digital Interface

Table 7. Band Bit Selection

Band Bits			
Bit 9	Bit 8	Selected Band	Band Range (MHz)
0	0	VHFL	30-90
0	1	VHFH	90.54-225
1	0	UHF	226.18-520
1	1	Unsupported, Do not Select	-

5.2 Example Tune Commands

Table 8. Example Tune Commands

$f_{DESIRED}$ (MHz)	Req. Band	Band (Hex)	f_{MIN} of Band (MHz)	f_{STEP} of Band (MHz)	f_{COM} Calculation (Decimal)	f_{COM} (Decimal)	f_{COM} (Hex)	Tune Command (Hex)
30.00	VHFL	0x00	30	0.24	$round\left(\frac{(30-30)}{0.24}\right)$	0	0x00	0x0000
47.25	VHFL	0x00	30	0.24	$round\left(\frac{(47.25-30)}{0.24}\right)$	72	0x48	0x0048
90.00	VHFL	0x00	30	0.24	$round\left(\frac{(90-30)}{0.24}\right)$	250	0xFA	0x00FA
90.54	VHFH	0x01	90.54	0.54	$round\left(\frac{(90.54-90.54)}{0.54}\right)$	0	0x00	0x0100
126.48	VHFH	0x01	90.54	0.54	$round\left(\frac{(126.48-90.54)}{0.54}\right)$	67	0x43	0x0143
225.00	VHFH	0x01	90.54	0.54	$round\left(\frac{(225.00-90.54)}{0.54}\right)$	249	0xF9	0x01F9
226.18	UHF	0x02	226.18	1.18	$round\left(\frac{(226.18-226.18)}{1.18}\right)$	0	0x00	0x0200
389.90	UHF	0x02	226.18	1.18	$round\left(\frac{(389.90-226.18)}{1.18}\right)$	139	0x8B	0x028B
520.00	UHF	0x02	226.18	1.18	$round\left(\frac{(520.00-226.18)}{1.18}\right)$	249	0xF9	0x02F9

5.3 Additional Interface Detail

Table 9. Additional Pin Information

Pin Name	Description
TUNE READY	Tune Ready Indicator – The TUNE READY pin is a driven digital output, do not connect any other push-pull output directly to this pin. The function of the TUNE READY pin is to indicate the status of the digital interface during/after tune events. The normal logic state of TUNE READY is low/de-asserted at power up. In this condition, the filter is ready to receive a new tune command. When a new tune command is initiated by pulling $\overline{CS}$ & $\overline{STB}$ low in serial mode or pulling $\overline{STB}$ low in parallel mode, the TUNE READY pin will transition high/assert after the filter is ready to start receiving digital data. The external control circuit must monitor the TUNE READY pin to determine when it transitions high or alternatively, delay for the minimum Control Circuit Setup Time before loading the digital data. Once the filter has received the valid tune command and has finished processing all tune functions, the TUNE READY pin will return to a logic low/de-asserted state. ***Note: In Parallel interface mode, if the TUNE READY pin is stuck high after completing a parallel tune, there is a chance that the control circuitry missed the second rising edge of $\overline{STB}$. If this happens transition $\overline{STB}$ low for > 300 ns and then back high. If the TUNE READY pin transitions low, the filter can be re-tuned.***
SER/$\overline{PAR}$	Serial/Parallel Command Interface Selection – The SER/$\overline{PAR}$ is sampled at power-up to determine which tune interface should be used to tune the filter. Leaving SER/$\overline{PAR}$ floating or pulled to V_{CC} will enable the SPI (serial) tune command interface. Keeping SER/$\overline{PAR}$ pulled to GND will enable the parallel tune command interface. Changes to interface modes will only take effect at power-up and cannot be changed on the fly. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
$\overline{CS}$ & $\overline{STB}$	SPI Chip Select and Tune Strobe – In Serial interface mode, $\overline{STB}$ wakes the control circuitry on a low transition. ***For proper operation in SPI mode, tie the $\overline{CS}$ (pin 8) and $\overline{STB}$ (pin 15) directly together externally or SPI mode will not function.*** In Parallel interface mode, $\overline{CS}$ is multiplexed with Parallel data A4. $\overline{STB}$ wakes the control circuitry on a low transition. The two subsequent rising edges of $\overline{STB}$ will load the most significant byte and least significant byte respectively.
TUNE MODE	Tune mode pin – The TUNE MODE pin is sampled at power-up to determine which tune mode should be used to tune the filter. Leave the TUNE MODE pin floating or pull to V_{CC} to enable legacy tune mode. Pull the TUNE MODE pin to ground to enable frequency weighted tune mode. Changes to the tune mode will only take effect at power-up and cannot be changed on the fly. (This pin is internally pulled to VCC with a 27 kΩ resistor.)

6.0 Tune Time

Tune times include internal processing of the tune command data and the 90% settled RF response time of the filter. This time excludes the time required to load the tune command into the filter. Low level signal measurements were utilized to show the Rx tune time that can be expected.

In addition, RF power in excess of +25 dBm is considered to be “hot switching” of the filter. While the data in “Table 11. Typical RF Tune Times” was taken via “hot switching”, this does not imply that tuning operation of the filter into these levels can be done reliably. It is recommended that RF is less than +20 dBm during a tune event.

Table 10. Typical RF Tune Times

Freq. (MHz)		Band	Input Power								Units
From	To		0	5	10	15	20	25	27	30	dBm
30	90	VHFL (0)	13.4	13.4	13.4	14.4	20.0	26.4	34.0	48.5	µs
90	30	VHFL (0)	17.6	17.6	17.6	17.6	17.6	17.6	17.6	17.6	
90.54	225	VHFH (1)	13.0	13.0	13.0	13.0	14.4	15.3	15.6	19.4	
225	90.54	VHFH (1)	16.6	16.6	16.6	16.6	16.6	16.6	16.6	16.6	
226.18	520	UHF (2)	10.6	10.6	10.6	10.7	10.9	11.4	12.0	14.0	
520	226.18	UHF (2)	16.4	16.4	16.4	16.4	16.4	16.4	16.4	16.4	
30	520	VHFL (0) to UHF (2)	14.0	14.0	14.0	14.0	14.0	15.5	15.5	15.5	
520	30	UHF (2) to VHFL (0)	17.4	17.4	17.4	17.8	18.6	19.0	19.0	19.2	

7.0 Application Information

7.1 Application Circuits

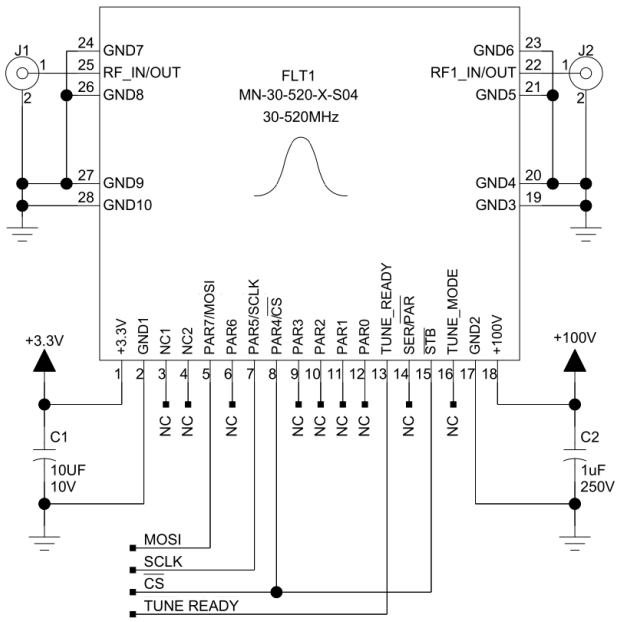


Figure 8. Serial Application Circuit

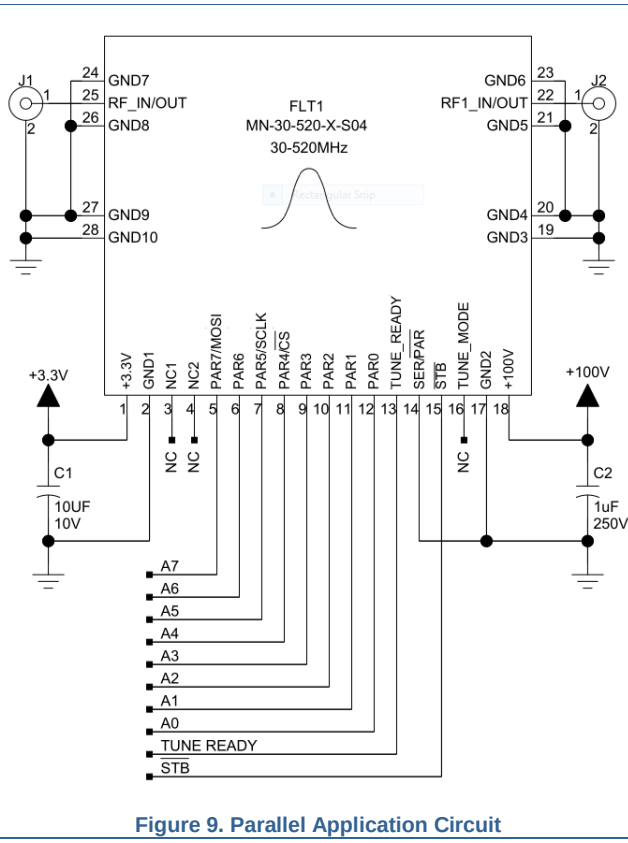


Figure 9. Parallel Application Circuit

8.0 Package Information

8.1 Package Detail

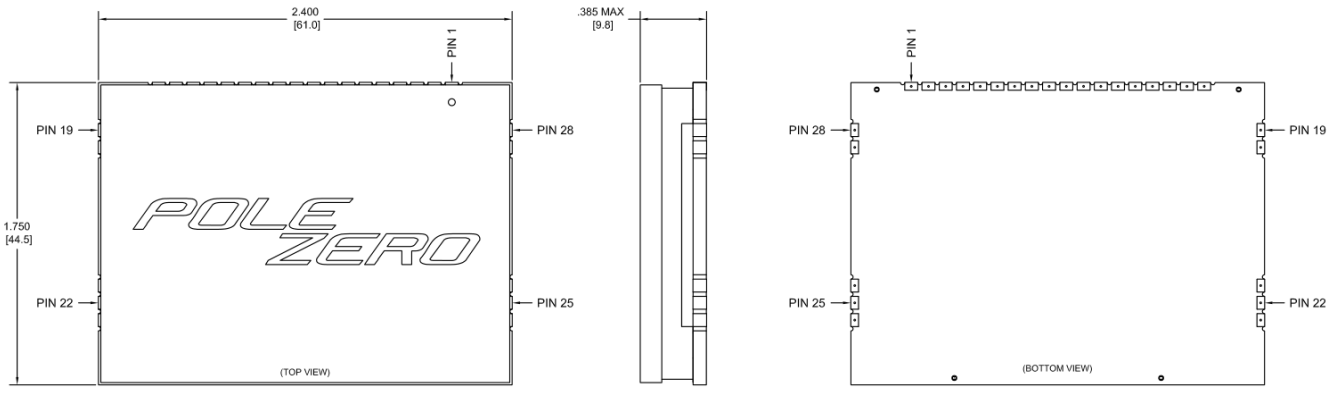


Figure 10. Package Detail

8.2 Recommended Pad Layout

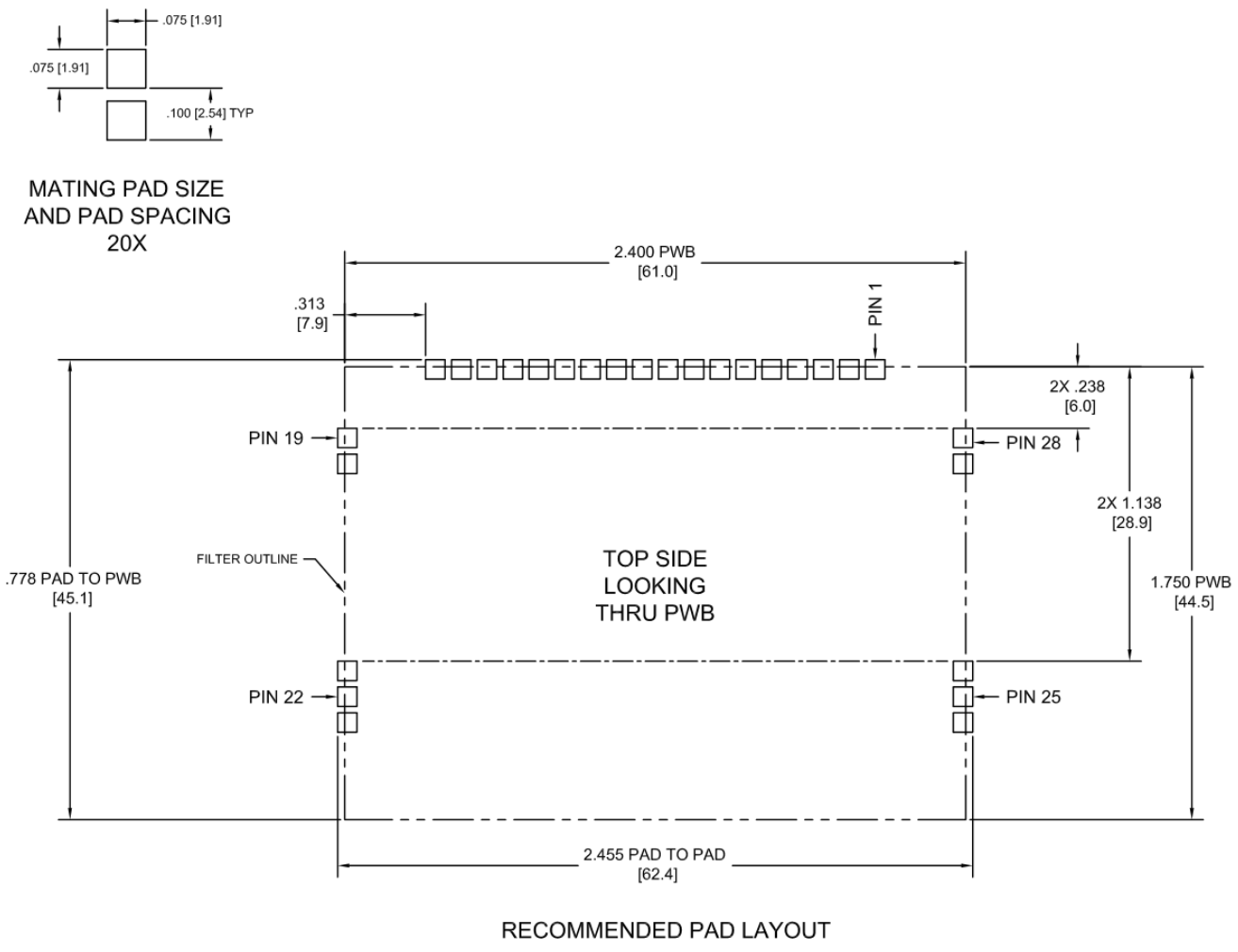


Figure 11. Recommended Pad Layout

9.0 Mounting Instructions

9.1 Solder Reflow Profile

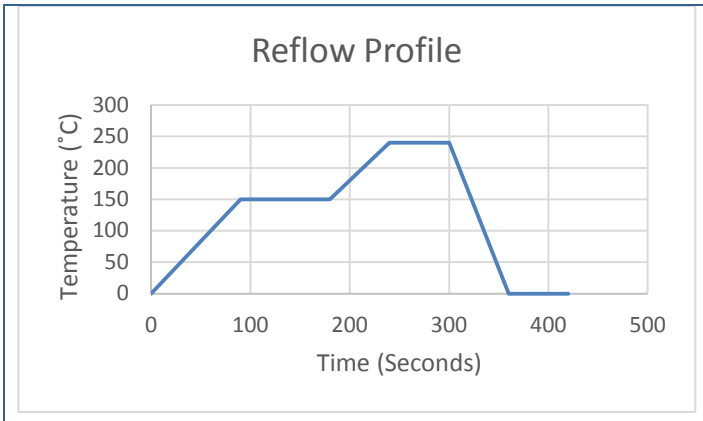


Figure 12. Recommended Solder Reflow Profile

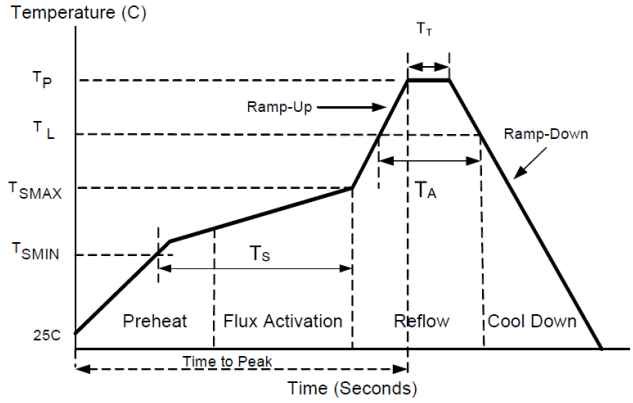


Figure 13. Reflow Profile Key

9.2 Temperature Options

Option	PWB Solder Mask Color	Reflowable?	Other Designators
High Temperature	Black	Yes	-
Standard Temperature	Green	No	-

9.3 Temperature Guidelines

9.3.1 Place the unit on the recommended layout pattern specified in this document in section **Error! Reference source not found.**. The parameters below describe the reflow profiles for Standard and Lead Free solder pastes. All temperatures are referenced to the PCB surface of the unit.

Parameter	Description	SAC305 Solder Paste	Sn63Pb37 Solder Paste
Ramp-up	Average ramp rate from T_{S_MAX} to T_P	3 °C/second average maximum	3 °C/second average maximum
T_{SMIN}	Preheat Peak Minimum	175 °C	150 °C
T_{SMAX}	Preheat Peak Minimum	200 °C	175 °C
T_P	Maximum Reflow Temperature	230 °C	225 °C
T_S	Time between T_{S_MAX} and T_{S_MIN}	75 – 120 seconds	45 – 90 seconds
T_L	Solder melting point	217 °C – 218 °C	183 °C
T_A	Time Above Liquidus (TAL)	60 – 120 seconds	45 – 90 seconds
T_T	Time within 5 °C of T_P	20 – 30 seconds	10 – 30 seconds
Ramp-Down	Ramp-down rate	6 °C per second maximum	6 °C per second maximum
Time to Peak	From 25 °C to peak temperature	270 seconds maximum	270 seconds maximum

9.4 Other Restrictions

9.4.1 Pole/Zero recommends a no-clean Sn63Pb37 solder paste.

9.4.2 If necessary to clean this product after assembly, Pole/Zero recommends the customer perform adequate experimentation to ensure their cleaning process is compatible with these filters.

9.4.3 Only subject the unit to one SMT reflow process.

9.4.4 Stencil thickness recommendation is between 0.005” and 0.008”.

9.4.5 Bake out process per J-STD-033B Package Thickness > 2.0 mm and ≤ 4.5 mm.

10.0 Safety Notes

10.1 Handling Information

Caution

This device contains electrostatic discharge sensitive devices and is sensitive to electrostatic discharge (ESD). Observe all precautions for handling electrostatic sensitive devices.

Caution

This device may produce potentially hazardous voltages. Take necessary precautions when handling this device while power is enabled.

Caution

This device is an MSL 4 component and should be packaged and handled according to the guidelines in J-STD-033.

11.0 Legal Information

11.1 Disclaimers

Limited warranty and liability – Information in this document is believed to be accurate and reliable. Pole/Zero and its suppliers disclaim all warranties, whether express or implied, including implied warranties of merchantability, fitness for a particular purpose, and non-infringement. The entire risk arising out of use or performance of this information remains with Licensee. Pole/Zero and its suppliers do not make any representations regarding the results of the use of the information in this document.

To the maximum extent permitted by applicable law, in no event will Pole/Zero or its directors, employees, distributors, licensors, suppliers, agents or resellers or suppliers (“Pole/Zero parties”) be liable for any indirect, special, incidental, consequential, or exemplary damages, even if such party has been advised of the possibility thereof. The Pole/Zero parties’ entire liability will not exceed the sum of the replacement of defective product or provision of a reasonably similar product, at Pole/Zero’s discretion. Some jurisdictions do not allow the exclusion or limitation of incidental, consequential or special damages, so this exclusion and limitation may not be applicable to Licensee. The Pole/Zero Parties will not be liable for any claims or damages arising out of content provided by Licensee.

11.2 Right to Make Changes

Pole/Zero Corporation reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

12.0 Learn More

For additional information, please visit http://www.dovermpg.com/polezero

13.0 Contact and Support

Pole/Zero Corporate Office
5558 Union Centre Drive
West Chester, OH 45069, USA
513-870-9060 (Phone)
513-870-9064 (Fax)