MN-X-X-X-S03, 700 - 3000 MHz, 1 Watt, High Performance Tunable Filter, MINI-filter®

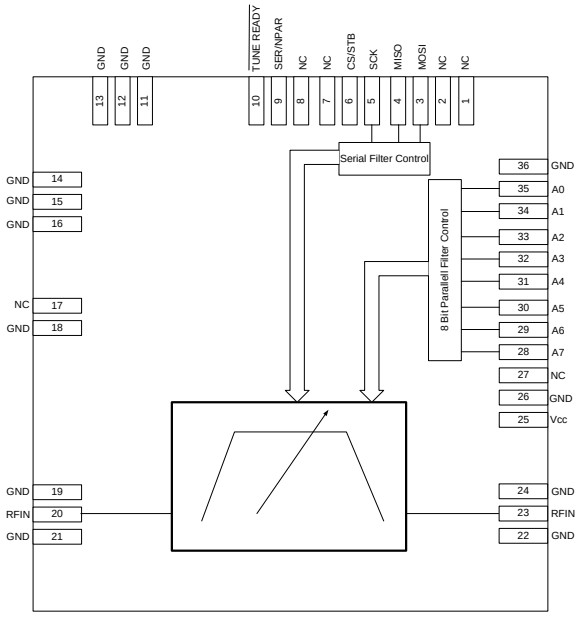
Typical Applications

- Applications where small size, high power, and high performance is needed.
- Military Handheld Radios
- Military Radar
- SATCOM and Space
- Test and Measurement Equipment
- Industrial and Medical Equipment

Features

- 1 Watt CW continuous Power handling
- +40 dBm IIP3
- Low IL (4 dB in a 5% filter)
- Good Selectivity (20 dB typ @ +/-10%)
- Fast Tune Time (4 μs)[1]

Functional Diagram



Description

MINI filters are low-cost, miniature, high-performance tunable bandpass filters. MINI filters use PIN diodes to deliver high filter performance while enclosed in a 1.5”x1.5”x0.25” package. Both serial and parallel tuning options are incorporated. All MINI filters are fully aligned and tested by Pole/Zero for convenience and ease of use.

[1] See Table 3 for more information.

1.0 Ordering Information

Table 1. Ordering Options

Series	-	Frequency Range (MHz)	-	% Bandwidth (3 dB)	-	Package
MN		700-1000		5		S03
MN		960-1240		3		S03
MN		1000-1500		5		S03
MN	-	1250-1850	-	5	-	S03
MN		1500-2000		5		S03
MN		2000-2500		5		S03
MN		2500-3000		5		S03

Note: Options may be limited to particular frequency bands and/or configurations. Consult Pole/Zero for your application.

Example product number: MN-700-1000-5-S03

2.0 Pinout and Functional Information

2.1 Pinout

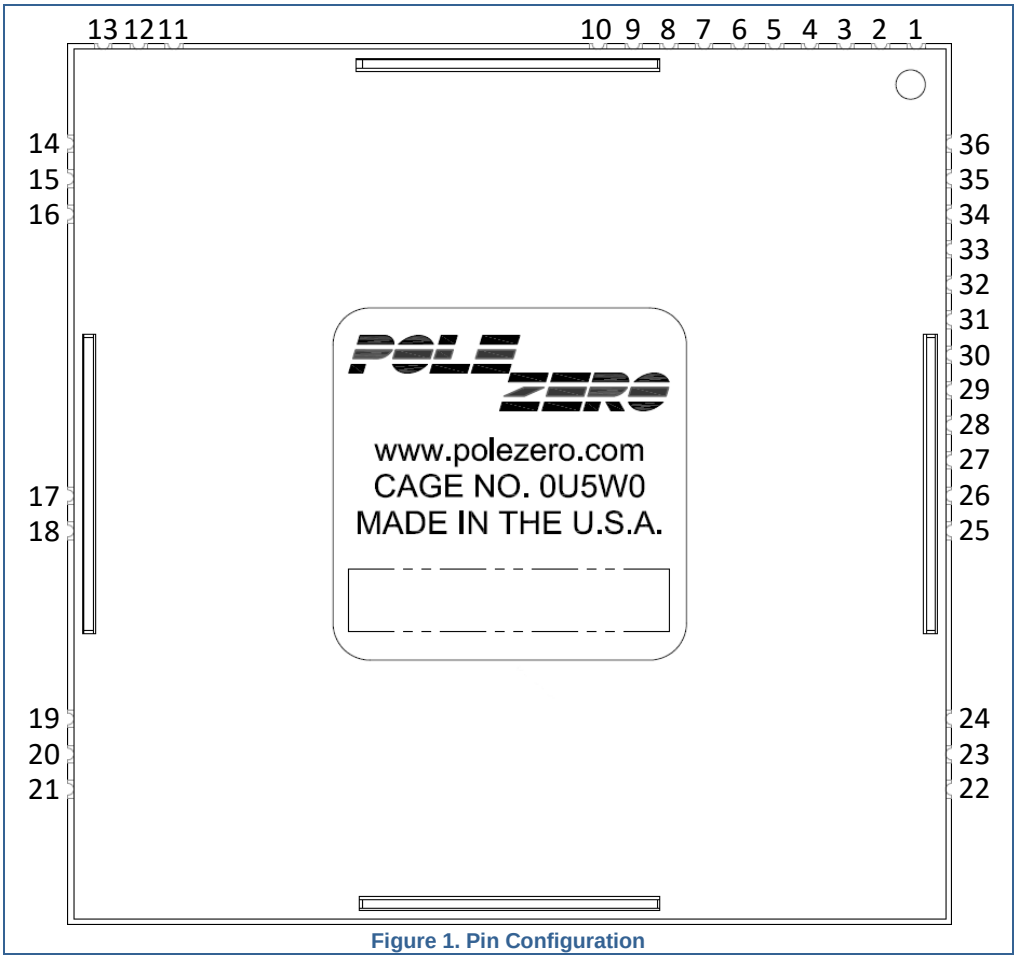


Figure 1. Pin Configuration

2.2 Pin Description

Table 2. Pin Functions and Descriptions

Pin Number	Label	Description
25	Vcc	Supply Voltage Input. 3.135 V ≤ V_{CC} ≤ 3.6 V.
11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 24, 26, 36	GND	Digital and Analog Ground.
1, 2, 7, 8, 17, 27	NC	No Connect. Shorting these pins may affect the performance and functionality of the filter. Please leave these pins floating. In an optional product configuration, the filter may have its internal high voltage bias supply circuit disabled, and pin 17 provides input connection for an external +100V bias supply.
20	RF_{IN}	RF Signal Input.
23	RF_{OUT}	RF Signal Output.
3	MOSI	SPI Master Out Slave In. Data is applied to MOSI for transferring tune commands to the device at the rising edge of SCK. The filter accepts input word lengths of 8 bits. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
4	MISO[2]	SPI Master In Slave Out.
5	SCK	SPI Clock. SCK is used to clock in the command data in SPI command mode. Data is latched on the rising edge. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
6	$\overline{CS}$/STB	In SPI mode: SPI Chip Select. When $\overline{CS}$/STB is taken low, the control circuitry wakes up and SCK is enabled for shifting data on MOSI into the filter. When $\overline{CS}$/STB is taken high, SCK is disabled and the specified tune command is executed. In Parallel mode: Data Strobe. When $\overline{CS}$/STB is taken low, the control circuitry wakes up and data is ready to be sent on A7-A0. When $\overline{CS}$/STB is taken high, the Parallel Data gets latched and the filter is commanded to the frequency specified by the Parallel Data interface. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
9	SER/$\overline{PAR}$	Serial/Parallel Command Interface Selection. Keeping SER/$\overline{PAR}$pulled to V_{CC} will enable the SPI tune command interface. Keeping SER/$\overline{PAR}$ pulled to GND will enable the Parallel tune command interface. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
10	$\overline{TUNE\ READY}$	Tune Ready Indicator. This pin normally remains high. When $\overline{CS}$/STB is taken low to initiate a tune in either SPI or Parallel tune modes, the $\overline{TUNE\ READY}$ pin transitions low to indicate the filter is ready to receive the SPI or Parallel tune command data. After data has been shifted in via the tune interface, the $\overline{TUNE\ READY}$ pin will transition back high indicating that the tune process is finishing.
28-35	A7-A0	Parallel Data Interface. Tune command bits which indicate which frequency the filter should tune to in Parallel tune command mode. A7 = MSB, A0 = LSB

[2] This pin is not used currently but may be used in the future to report status information.

3.0 Specifications

3.1 Absolute Maximum Ratings[3]

Voltages are referenced to GND (ground = 0V). Operating at room temperature (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	-	-0.3	4	V
V_I	Input voltage	On all digital interface input pins	-0.5	Vcc + 0.5	V
V_O	Output voltage	On all digital interface output pins	-0.5	Vcc + 0.5	V
I_{OH}/I_{OL}	Digital interface pin sink/source current	-	-25	25	mA
P_{INBAND}	In-band RF input power level	Signal is in passband $f_0 = 700 - 3000MHz$	-	32	dBm
$P_{OUTBAND}$	Out-of-band RF input power level	-	-	33	dBm
T_{RATE}	Maximum tune rate (frequency hopping)	-	-	8.4	kHz

3.2 Handling Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
T_S	Storage temperature	-	-40	125	°C

3.3 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{CC}	Supply voltage	-	3.135	3.3	3.6	V
P_{IN}	Maximum RF input power for linear operation	Signal is in passband	-	-	30	dBm
T_A	Ambient operating temperature	-	-40	-	85	°C

3.4 Electrical Characteristics

All specifications at T_A = 23 °C, V_{cc} = 3.3 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_{CC_STATIC}	V_{CC} current consumption, statically tuned	At nominal V_{CC} voltage	-	150	230	mA
I_{CC_HOP}	V_{CC} current consumption, hopping	Nominal V_{CC}, hopping at 8.4kHz	-	-	260	mA
V_{IH}	Digital high level input voltage	On all digital interface input pins	0.7 * Vcc	-	-	V
V_{IL}	Digital low level input voltage	On all digital interface output pins	-	-	0.3 * Vcc	V
F_{RANGE}[4]	Tunable frequency range	-	-	-	-	MHz
Z_O	Input/output impedance	-	-	50	-	Ω
VSWR	Voltage Standing Wave Ratio	-	-	1.92		-

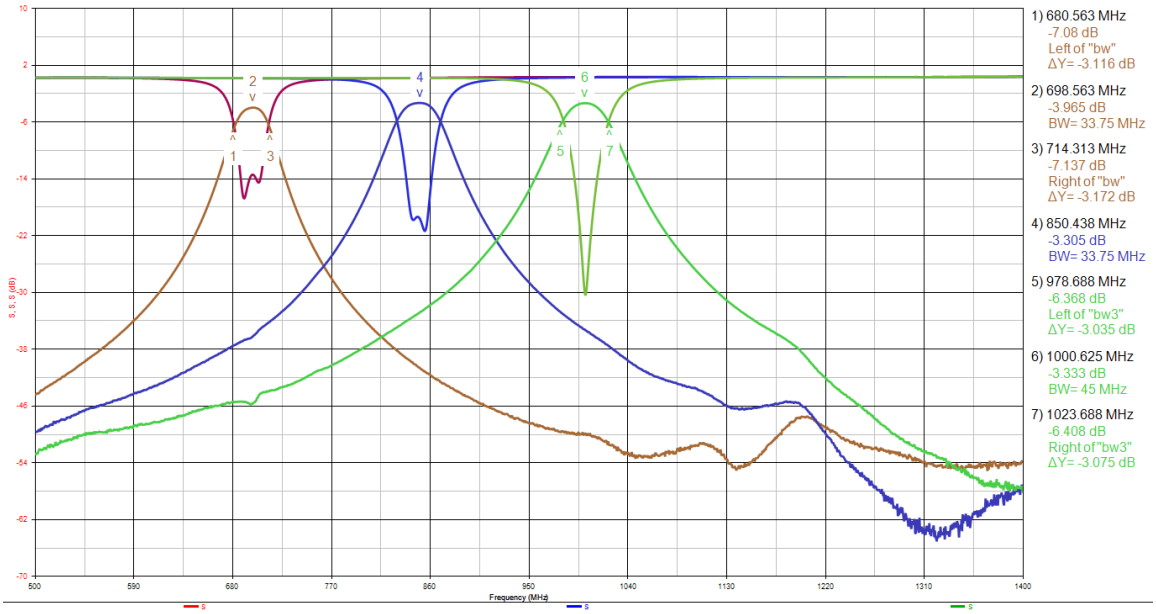
[3] Maximum operating conditions before damage occurs.

[4] Varies depending on frequency range and bandwidth of selected unit.

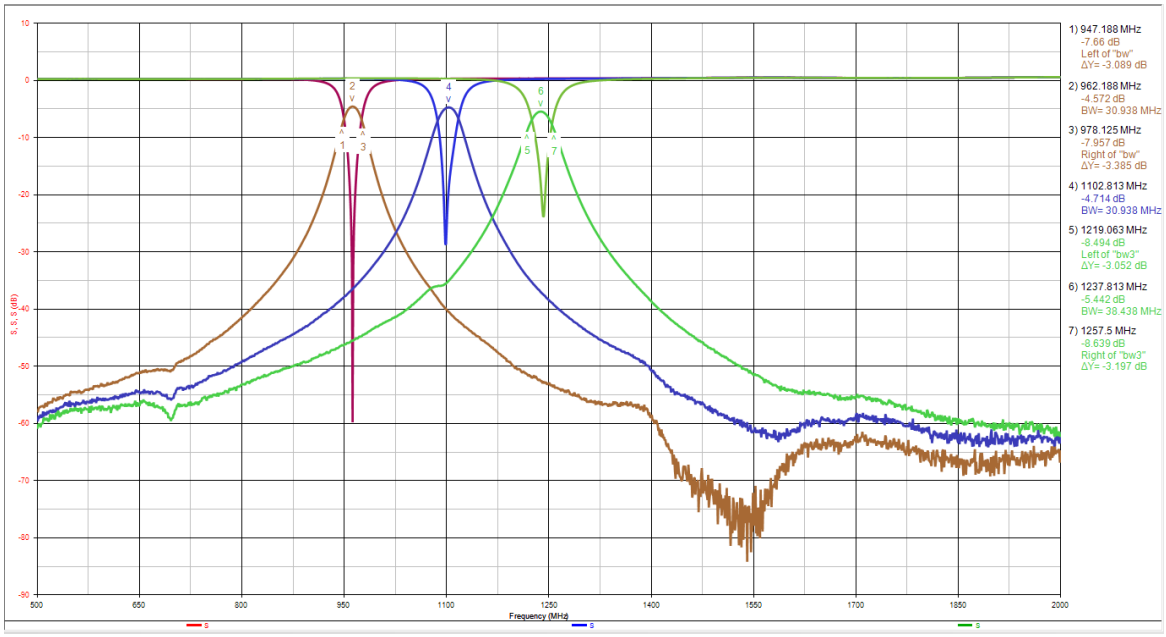
Symbol	Parameter	Conditions	Min	Nom	Max	Unit
RL	Return loss	At 50 Ω	10	15	-	dB
IL[4]	Insertion loss	-	-	4	-	dB
BW	Bandwidth (3 dB)	MN-X-X-3-S03	-	3	-	%
		MN-X-X-5-S03		5		
$SEL_{10\%}$	Selectivity 10% removed from the center frequency	$f_o \pm 10\%$	17	20	-	dBc
$SEL_{ULTIMATE}$	Ultimate selectivity	$2 \times f_o$	-	40	-	dBc
IIP3	Input third order intermodulation intercept point	-	40	45	-	dBm
NF	Noise figure	-	-	IL	TBD	dB
$T_{TUNE\ (Serial)}$[5]	Tune time	-	-	4	-	µs
F_{DRIFT}	Center frequency drift over temperature		-40	-	85	ppm/°C

[5] See Tune Time section

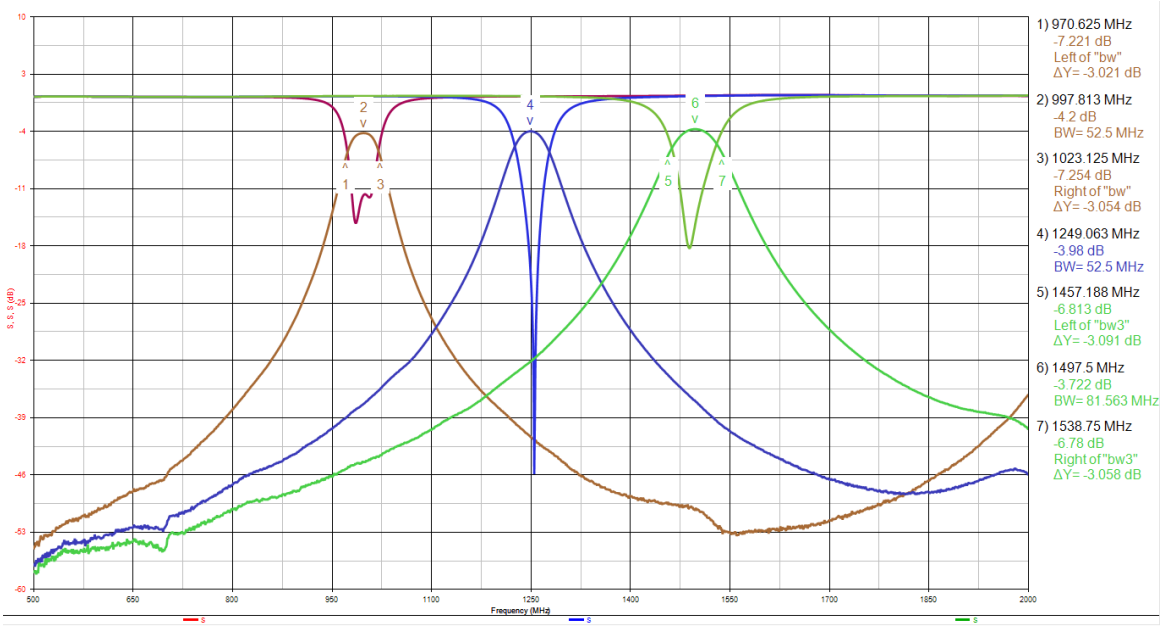
3.5 Typical Characteristics



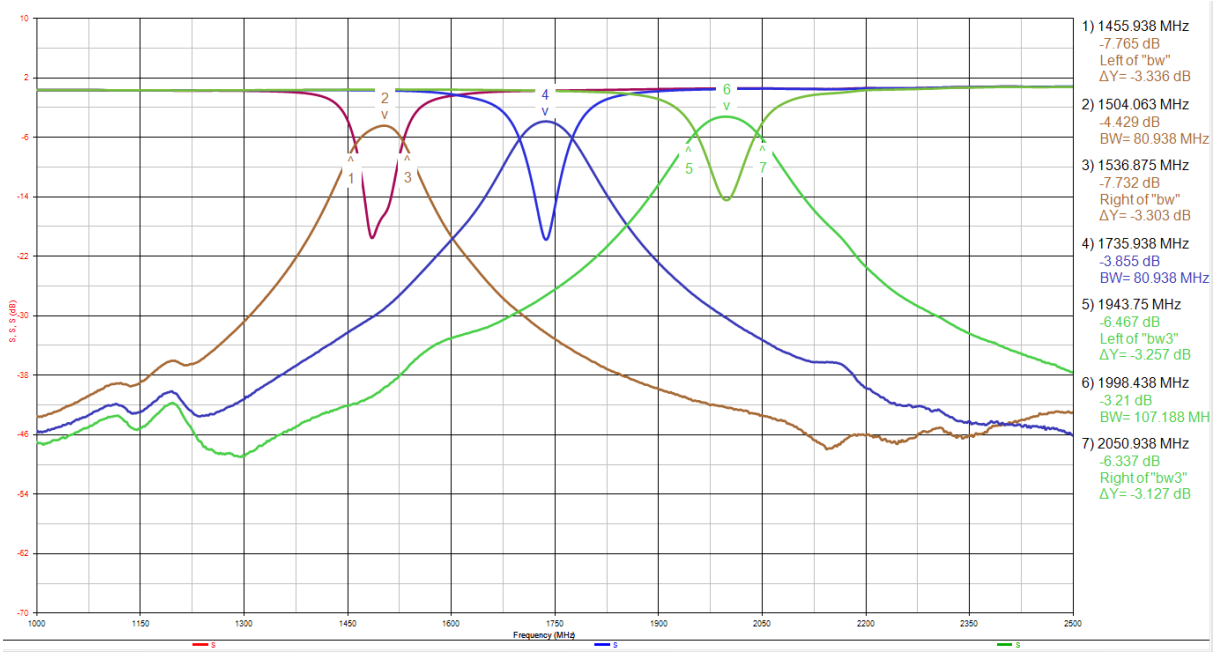
Model: 700 – 1000MHz, 5% BW



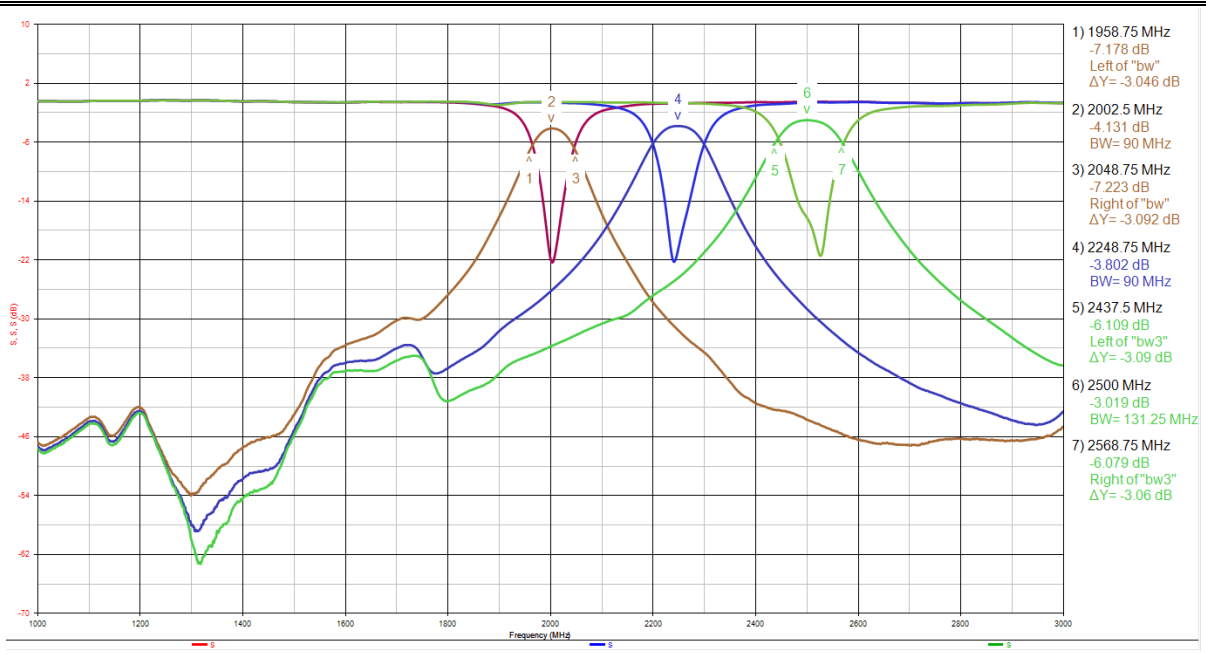
Model: 960 – 1240MHz, 3% BW



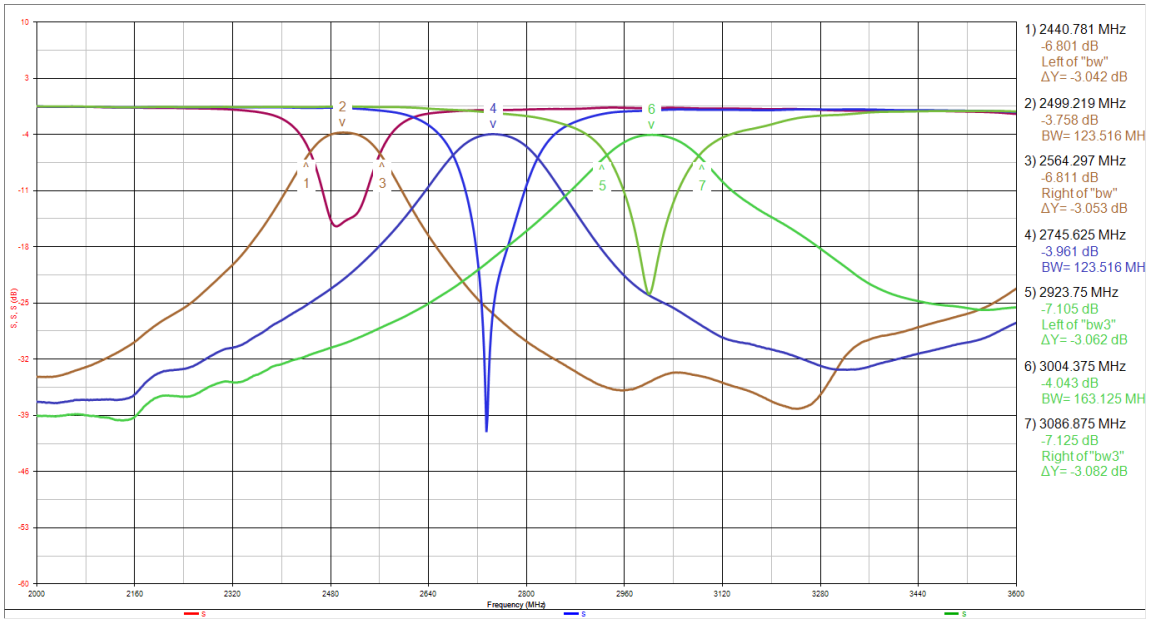
Model: 1000 – 1500 MHz, 5% BW



Model: 1500 – 2000 MHz, 5% BW



Model: 2000 – 2500 MHz, 5% BW



Model: 2500 – 3000 MHz, 5% BW

3.6 Timing Requirements

3.6.1 SPI Interface Timing

The SPI tune command interface is a standard SPI interface with Mode = 0 (CPOL = 0, CPHA = 0). There are always 8 data bits. Any bits that do not affect the frequency offset of the filter should always be set to 0. The interface receives the data most significant bit first.

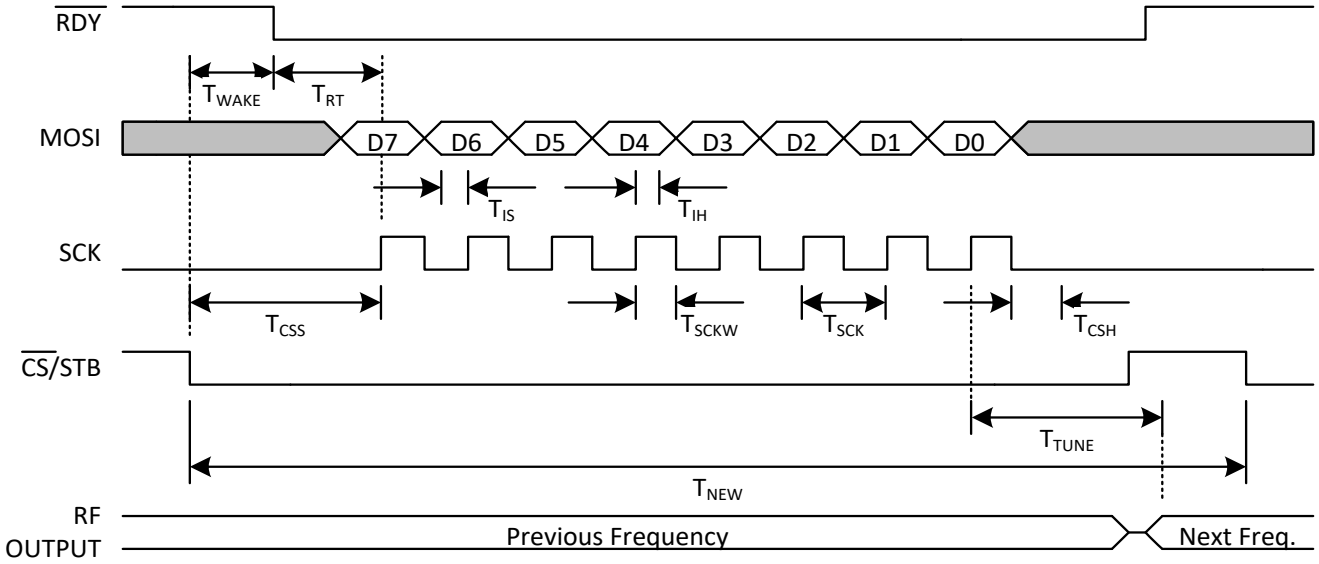


Figure 2. Serial Timing Diagram

Table 3. SPI Timing Characteristics

V_{CC} = 3.3 V +/-5%, GND = 0 V

Parameter	Parameter	Min.	Max.	Unit
T_{WAKE}	Wakeup Time – The amount of time from $\overline{CS}$/STB transitioning low until $\overline{TUNE\ READY}$ transitions low.	-	6.5	µs
T_{RT}	Ready to Tune Time – Time needed after $\overline{TUNE\ READY}$ transitions low before a rising edge of SCK can be sent.	600	-	ns
T_{IS}	MOSI Setup SCK – The amount of time data needs to be valid on MOSI before the rising edge of SCK.	10	-	ns
T_{IH}	MOSI Hold SCK – The amount of time data needs to be valid on MOSI after the rising edge of SCK.	10	-	ns
T_{CSS}	$\overline{CS}$/STB Setup Time – If not polling the $\overline{TUNE\ READY}$ pin, the minimum amount of time needed from when $\overline{CS}$/STB transitions low until the first rising edge of SCK.	7.1	-	µs
T_{SCKW}	SCK Duty Cycle – Duty cycle of the SPI clock.	$\frac{T_{SCK}}{2}$	-	ns
T_{SCK}	SCK Period – Period of the SPI clock.	125	-	ns
T_{CSH}	$\overline{CS}$/STB Hold Time – The amount of time $\overline{CS}$/STB needs to remain low after the last falling edge of SCLK.	50	-	ns
T_{NEW}	New Command Delay – The amount of between falling edges of $\overline{CS}$/STB. This is the time between the start of new tune commands.	120	-	µs
T_{TUNE}	Tune Time – Time from the last clock of data on the SPI interface until the RF response reaches 90% of the commanded frequency.	-	~4 [6]	µs

[6] See section 6.0 Tune Time to see typical tune time numbers.

3.6.2 Parallel Interface Timing

The Parallel tune command interface is an 8-bit synchronous parallel interface. There are always 8 data bits. Any bits that do not affect the frequency offset of the filter should always be set to 0. A7 is the MSB and A0 is the LSB.

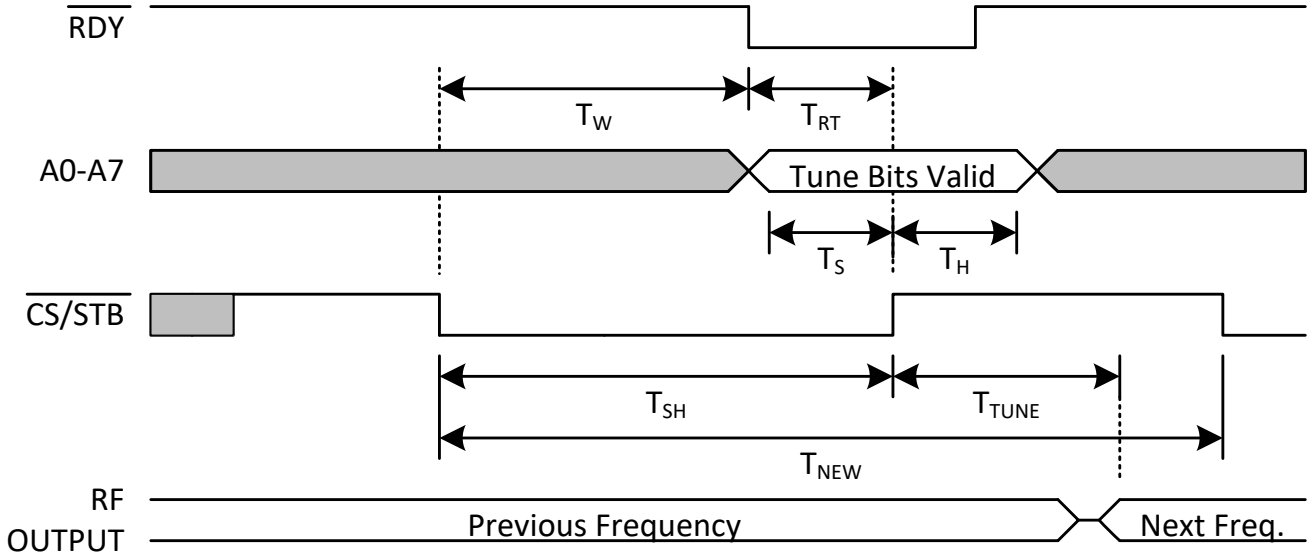


Figure 3. Parallel Timing Diagram

Table 4. Parallel Timing Characteristics

V_{CC} = 3.3 V +/-5%, GND = 0 V

Symbol	Parameter	Min.	Max.	Unit
T_W	Wakeup Time – The amount of time from $\overline{CS}$/STB transitioning low until $\overline{TUNE\ READY}$ transitions low.	-	6.5	µs
T_{RT}	Ready to Tune Time – The amount of time needed to wait after $\overline{TUNE\ READY}$ transitions low and before a rising edge of $\overline{CS}$/STB can be sent.	600	-	ns
T_S	Parallel Command Setup Time – The amount of time the command data needs to be present and valid before $\overline{CS}$/STB transitioning high.	300	-	ns
T_H	Parallel Command Hold Time – The amount of time the command data needs to be present and valid after $\overline{CS}$/STB transitions high.	300	-	ns
T_{NEW}	New Command Delay – The amount of time after $\overline{TUNE\ READY}$ has transitioned back high needed to wait before sending a new tune command.	120	-	µs
T_{SH}	Strobe Hold Time – If not polling the $\overline{TUNE\ READY}$ pin, the minimum amount of time needed to hold the strobe pin low before loading the data on the rising edge.	7.1	-	µs
T_{TUNE}	Tune Time – Time from the rising edge of $\overline{CS}$/STB until the RF response reaches 90% of the commanded frequency.	-	~4 [7]	µs

[7] See section 6.0 Tune Time to see typical tune time numbers.

4.0 Functional Description

4.1 Tune Commands

Table 5. Tune Command Properties

Symbol	Value	Description
f_{MIN}	See part series below	Minimum Tunable Frequency. f_{MIN} is the absolute minimum frequency that the filter is capable of tuning to for the respective band.
f_{MAX}	See part series below	Maximum Tunable Frequency. f_{MAX} is the absolute maximum frequency that the filter is capable of tuning to. Sending tune commands greater than the maximum tunable frequency will result in an invalid tune condition. The frequency response of an invalid tune is unknown. Normal frequency response will return on the next valid tune command. Varies depending on the band.
f_{STEP}	See part series below	Tune step size. f_{STEP} is the minimum spacing between adjacent tune commands.
f_{COM}	$round\left(\frac{(f_{DESIRED} - f_{MIN})}{f_{STEP}}\right)$	Commanded Frequency. f_{COM} is the commanded frequency that is sent over the SPI or parallel tune interface. The command can be calculated by subtracting f_{MIN} from the desired frequency for the particular band, dividing the result by the f_{STEP} of that band, and then rounding to the nearest integer command. The formula is used to select the closest possible frequency to the desired tune word. If the next lowest tune word is desired, replace the round operation with floor and if the next highest tune word is desired replace the round operation with ceil.

Table 6. Tune Command Format

Filter Model											
Part Series	f_{MIN} (MHz)	f_{MAX} (MHz)	f_{STEP} (MHz)	(MSB) 7	6	5	4	3	2	1	(LSB) 0
MN-700-1000-5-S03	700	1000	2	256	128	64	32	16	8	4	2
MN-960-1240-3-S03	960	1240	2	256	128	64	32	16	8	4	2
MN-1000-1500-5-S03	1000	1500	2	256	128	64	32	16	8	4	2
MN-1250-1850-5-S03	1250	1850	2.4	307.2	153.6	76.8	38.4	19.2	9.6	4.8	2.4
MN-1500-2000-5-S03	1500	2000	5	N/A[8]	320	160	80	40	20	10	5
MN-2000-2500-5-S03	2000	2500	10	N/A	N/A	320	160	80	40	20	10
MN-2500-3000-5-S03	2500	3000	10	N/A	N/A	320	160	80	40	20	10

[8] Any bit marked as N/A should be loaded into the unit as a zero.

5.0 Detailed Description

5.1 Example Tune Commands

Table 7. Example Tune Commands

$f_{DESIRED}$ (MHz)	f_{STEP} of Filter (MHz)	f_{COM} Calculation (Decimal)	f_{COM} (Decimal)	Tune Command (Hex)
MN-700-1000-X-S03 Examples				
700	2	$round\left(\frac{(700-700)}{2}\right)$	0	0x00
900	2	$round\left(\frac{(900-700)}{2}\right)$	100	0x64
1000	2	$round\left(\frac{(1000-700)}{2}\right)$	150	0x96
MN-960-1240-X-S03				
960	2	$round\left(\frac{(960-960)}{2}\right)$	0	0x00
1100	2	$round\left(\frac{(1100-960)}{2}\right)$	70	0x46
1240	2	$round\left(\frac{(1240-960)}{2}\right)$	140	0x8C
MN-1000-1500-X-S03				
1000	2	$round\left(\frac{(1000-1000)}{2}\right)$	0	0x00
1250	2	$round\left(\frac{(1250-1000)}{2}\right)$	125	0x7D
1500	2	$round\left(\frac{(1500-1000)}{2}\right)$	250	0xFA
MN-1250-1850-X-S03				
1250	2.4	$round\left(\frac{(1250-1250)}{2.4}\right)$	0	0x00
1550	2.4	$round\left(\frac{(1550-1250)}{2.4}\right)$	125	0x7D
1850	2.4	$round\left(\frac{(1850-1250)}{2.4}\right)$	250	0xFA
MN-1500-2000-X-S03				
1500	5	$round\left(\frac{(1500-1500)}{5}\right)$	0	0x00
1750	5	$round\left(\frac{(1750-1500)}{5}\right)$	50	0x32
2000	5	$round\left(\frac{(2000-1500)}{5}\right)$	100	0x64
MN-2000-2500-X-S03				
2000	10	$round\left(\frac{(2000-2000)}{10}\right)$	0	0x00
2250	10	$round\left(\frac{(2250-2000)}{10}\right)$	25	0x19
2500	10	$round\left(\frac{(2500-2000)}{10}\right)$	50	0x32
MN-2500-3000-X-S03				
2500	10	$round\left(\frac{(2500-2500)}{10}\right)$	0	0x00
2750	10	$round\left(\frac{(2750-2500)}{10}\right)$	25	0x19
3000	10	$round\left(\frac{(3000-2500)}{10}\right)$	50	0x32

5.2 Additional Interface Detail

Table 8. Additional Pin Information

Pin Name	Description
$\overline{\text{TUNE READY}}$	Tune Ready Indicator – The $\overline{\text{TUNE READY}}$ pin is a driven digital output, do not connect any other push-pull output directly to this pin. The function of the $\overline{\text{TUNE READY}}$ pin is to indicate the status of the digital interface during/after tune events. The normal logic state of $\overline{\text{TUNE READY}}$ is high/de-asserted at power up. In this condition, the filter is ready to receive a new tune command. When a new tune command is initiated by pulling $\overline{\text{CS}}$/STB low, the $\overline{\text{TUNE READY}}$ pin will transition low/assert after the filter is ready to start receiving digital data. The external control circuit must monitor the $\overline{\text{TUNE READY}}$ pin to determine when it transitions low or alternatively, delay for the minimum Control Circuit Setup Time before loading the digital data. Once the filter has received the valid tune command and has finished processing all tune functions, the $\overline{\text{TUNE READY}}$ pin will return to a logic high/de-asserted state.
SER/$\overline{\text{PAR}}$	Serial/Parallel Command Interface Selection – The SER/$\overline{\text{PAR}}$ is sampled at power-up to determine which tune interface should be used to tune the filter. Leaving SER/$\overline{\text{PAR}}$ floating or pulled to V_{CC} will enable the SPI (serial) tune command interface. Keeping SER/$\overline{\text{PAR}}$ pulled to GND will enable the parallel tune command interface. Changes to interface modes will only take effect at power-up and cannot be changed on the fly. (This pin is internally pulled to VCC with a 27 kΩ resistor.)
$\overline{\text{CS}}$/STB	SPI Chip Select and Tune Strobe – The $\overline{\text{CS}}$/STB pin serves two functions: to start up the necessary internal clock circuitry used during tuning and to command the filter to load the tune word. The normal state of $\overline{\text{CS}}$/STB should be asserted to logic high in serial and parallel mode. A new tune event is initiated by setting the $\overline{\text{CS}}$/STB pin low. When the filter is set for serial mode (by asserting the SER/$\overline{\text{PAR}}$ pin), the $\overline{\text{CS}}$/STB pin should be de-asserted to logic low while the data is shifted into the filter. $\overline{\text{CS}}$/STB should be asserted high at the end of an SPI tune data to complete the tune. Signal timing can be seen in section 3.6.1 SPI Interface Timing. When the filter is set for parallel mode (by de-asserting the SER/$\overline{\text{PAR}}$ pin), the $\overline{\text{CS}}$/STB pin should be de-asserted to initiate a new tune event and then asserted to latch the parallel data lines. Signal timing can be seen in section 3.6.2 Parallel Interface Timing. It is recommended that $\overline{\text{CS}}$/STB is asserted high during power up. This will ensure that the filter will be in the proper state to receive the first tune command. (This pin is internally pulled to VCC with a 27 kΩ resistor.)

6.0 Tune Time

Tune times include internal processing of the tune command data and the 90% settled RF amplitude response time of the filter. This time excludes the time required to load the tune command into the filter. Low level signal measurements were utilized to show the receive tune time that can be expected. In addition, RF power in excess of +25 dBm is considered to be “hot switching” of the filter. It is recommended that RF is less than +20 dBm during a tune event. All of the tune times listed in Table 9. Typical RF Tune Times, were taken with the input RF power set to +10 dBm.

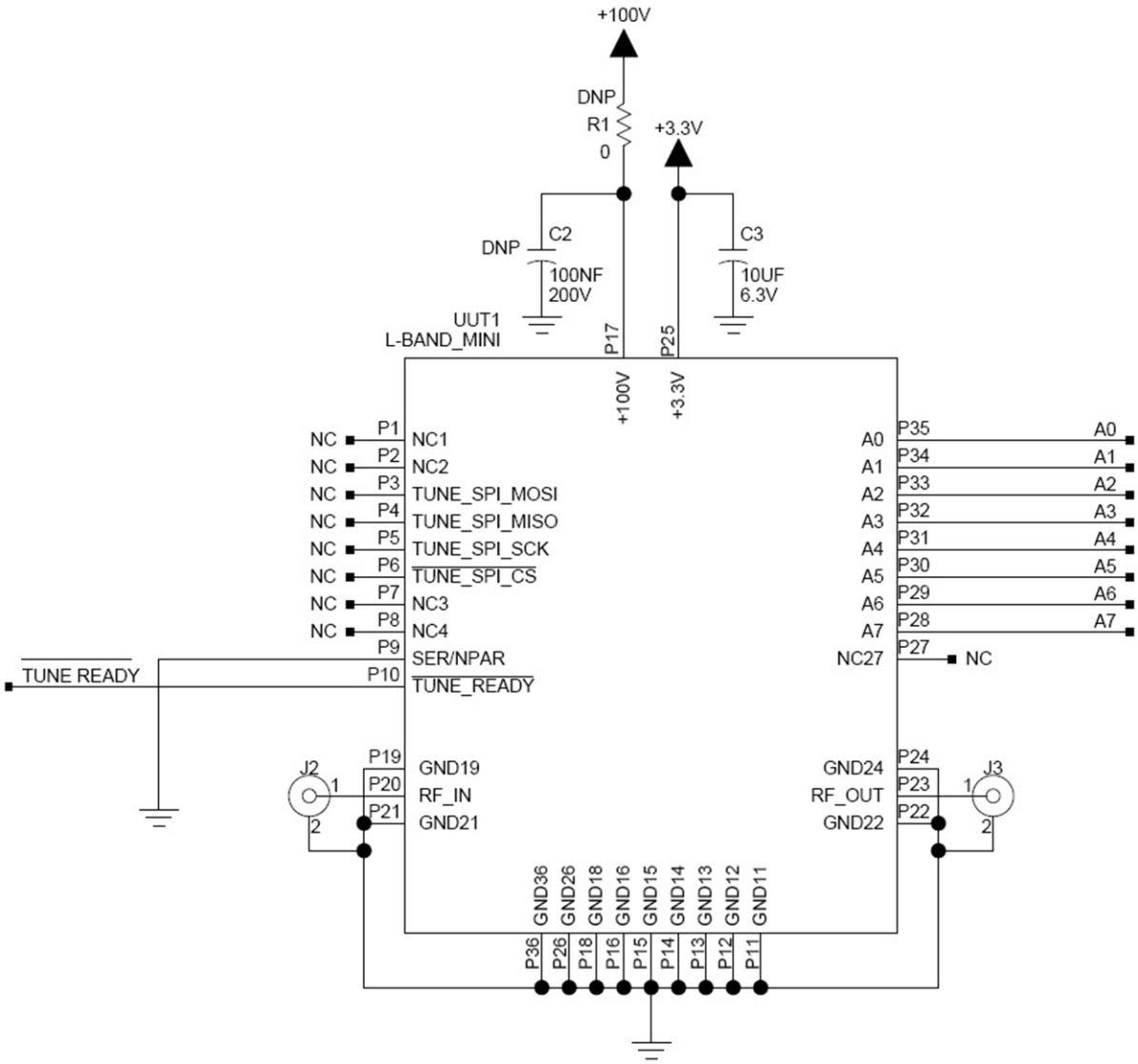
Table 9. Typical RF Tune Times

Freq. (MHz) From	Freq. (MHz) To	Catalog Part Number	Tune Time (µs)
700	1000	MN-700-1000-X-S03	3.6
960	1240	MN-960-1240-X-S03	3.55
1000	1500	MN-1000-1500-X-S03	3.68
1250	1850	MN-1250-1850-X-S03	4.0[9]
1500	2000	MN-1500-2000-X-S03	3.86
2000	2500	MN-2000-2500-X-S03	3.9
2500	3000	MN-2500-3000-X-S03	3.76

[9] No measured data available at this time for this part number. Tune time estimated to be 4.0 µs or less.

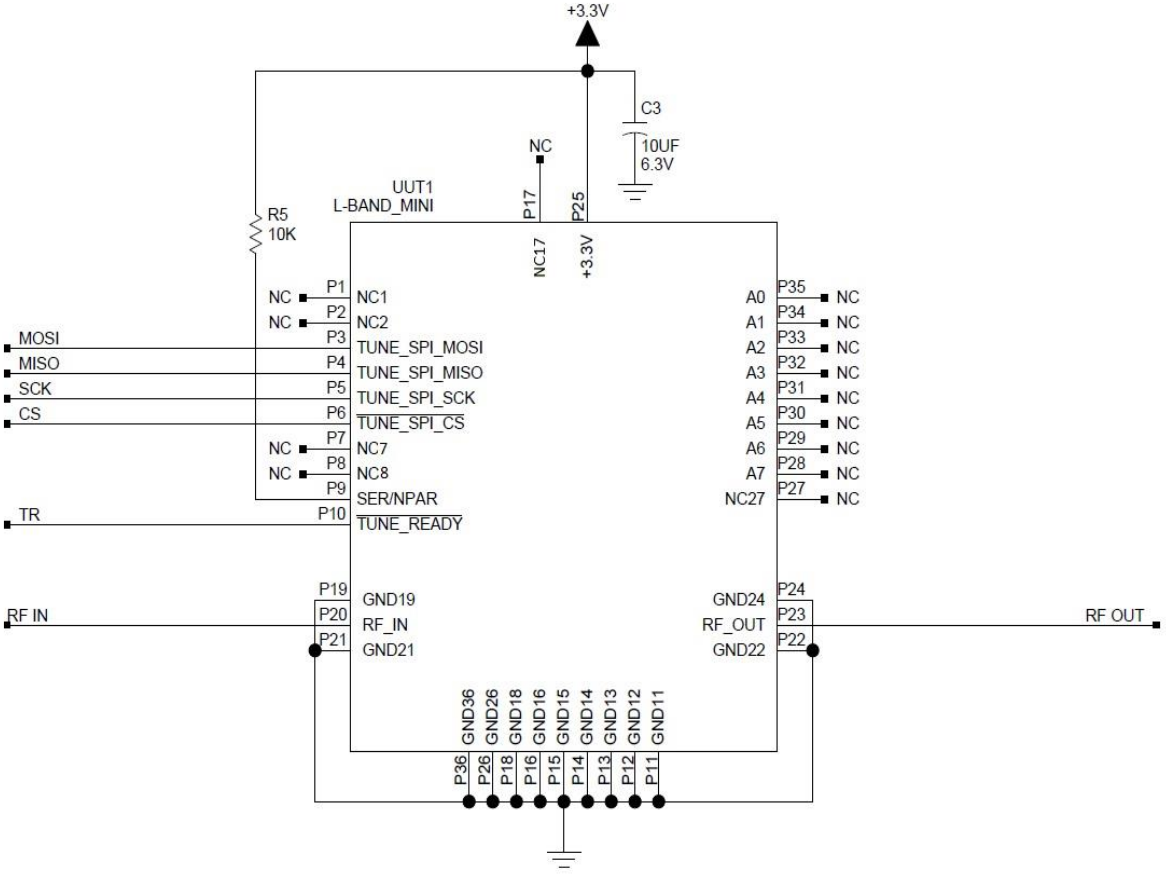
7.0 Application Information

7.1 Application Circuits



Parallel Connection Schematic

Note: For the standard product configuration, do not connect Pin 17. In an optional product configuration that must be specified when ordering, the filter may have its internal high voltage bias supply circuit disabled, and pin 17 provides input connection for an external +100V bias supply. This optional configuration is shown in the reference schematic, above.



Serial Connection Schematic

Note: The standard configuration with pin 17 as a No Connect is shown in the serial control schematic above.

8.0 Package Information

8.1 Package Detail

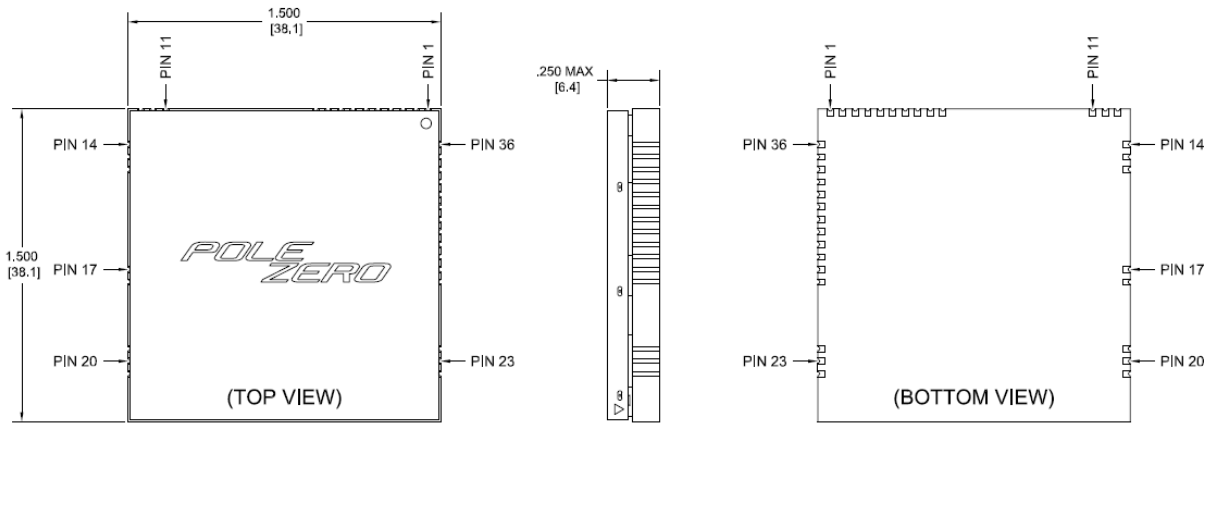


Figure 4. Package Detail

8.2 Recommended Pad Layout

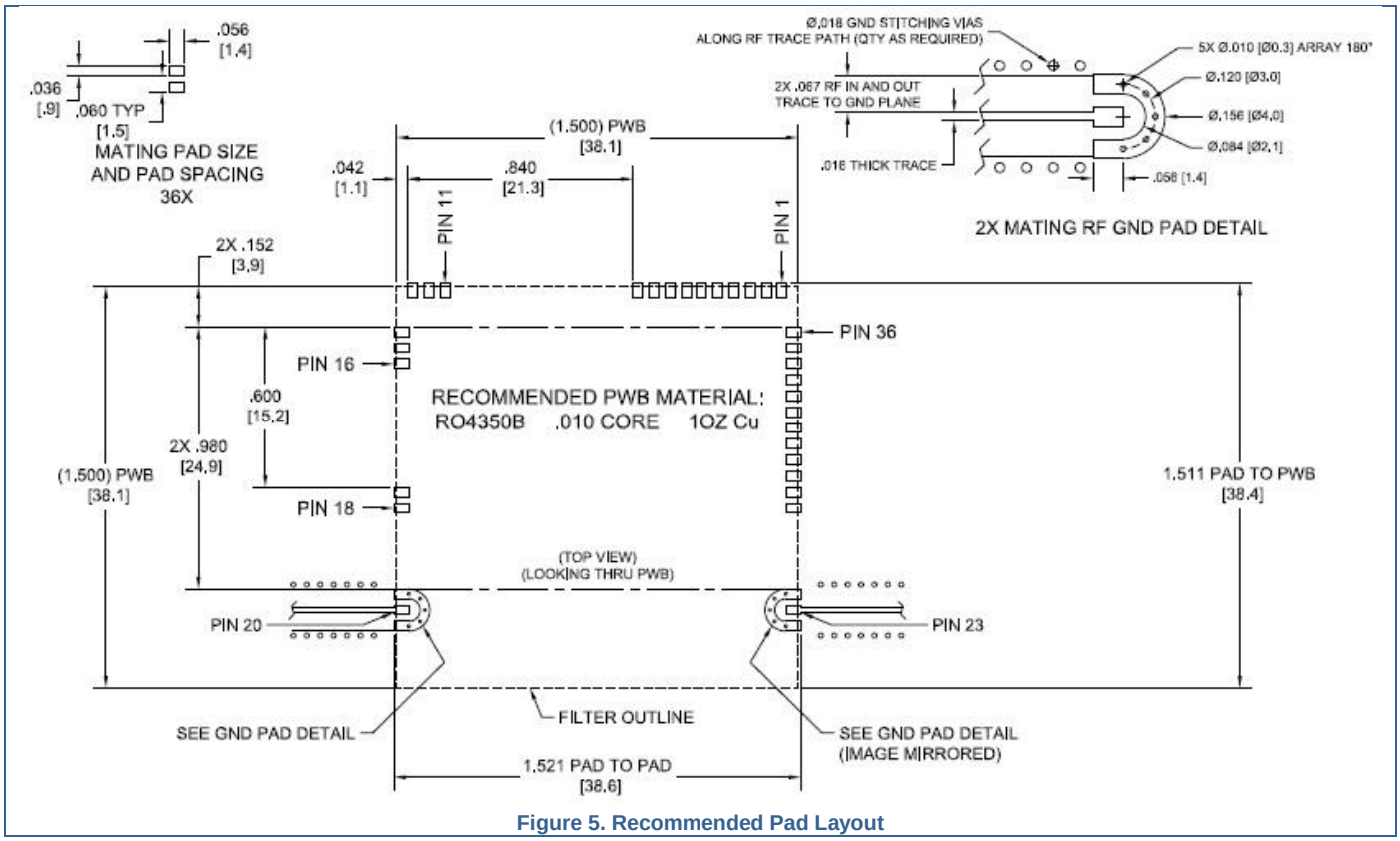


Figure 5. Recommended Pad Layout

9.0 Safety Notes

9.1 Handling Information

Caution

This device contains electrostatic discharge sensitive devices and is sensitive to electrostatic discharge (ESD). Observe all precautions for handling electrostatic sensitive devices.

Caution

This device may produce potentially hazardous voltages. Take necessary precautions when handling this device while power is enabled.

Caution

This device is an MSL 4 component and should be packaged and handled according to the guidelines in J-STD-033.

10.0 Legal Information

10.1 Disclaimers

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11.0 Learn More

For additional information, visit http://www.dovermpg.com/polezero and navigate to the MINI-SMT® product page.

12.0 Contact and Support

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